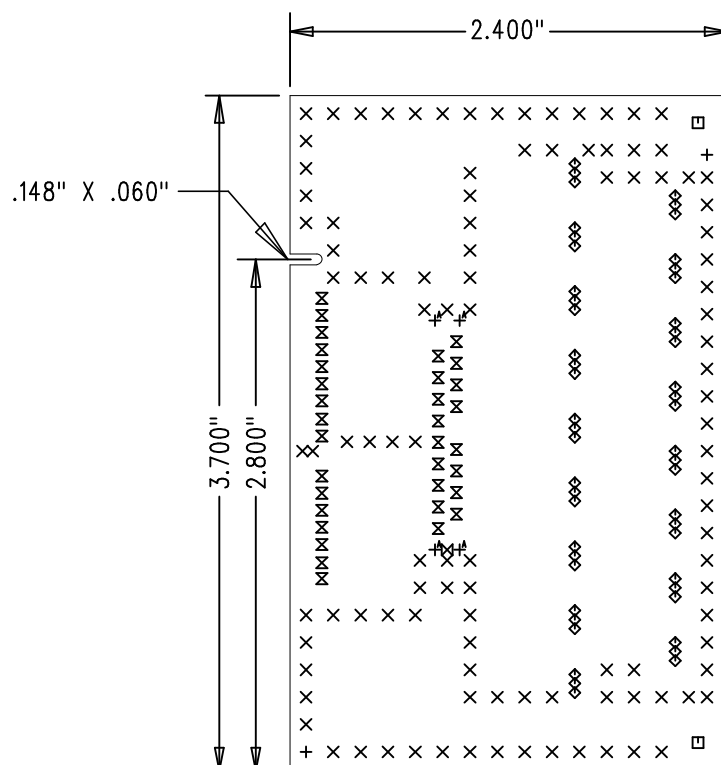


REVISION HISTORY				
ECO	REV	DESCRIPTION	APP. ENG.	DATE
-	2	PRODUCTION	MARK T.	03-04-10



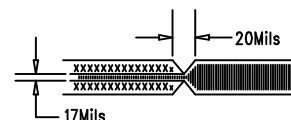
LINEAR TECHNOLOGY DRILL DRAWING LAYER  
DC1321A  
ADC LOGIC PROBE ADAPTER BOARD  
DATE: 03-04-10

SIZE	QTY	SYM	PLATED	TOL
0.072	2	+	NO	+/-0.003
0.02	109	X	YES	+/-0.003
0.187	2	□	NO	+/-0.003
0.023	51	◇	YES	+/-0.003
0.008	33	⊗	YES	+/-0.003
0.035	1	⊗	NO	+/-0.003
0.028	4	⊕ <sup>A</sup>	YES	+/-0.003

4 LAYERS	7	.0028"	Microstrip
	7	.012"	Prepreg
	7	.0014"	Microstrip
	7	.0014"	Core Material
4 LAYERS	7	.0014"	Microstrip
	7	.012"	Prepreg
	7	.0028"	Microstrip
	7	.0028"	Microstrip

## NOTES: UNLESS OTHERWISE SPECIFIED:

- FAB PER IPC-A-600, PCBS ARE TO BE RoHS COMPLIANT
- MATERIAL: EPOXY FIBERGLASS, NEMA GRADE FR-4, 4 LAYERS  
FINISHED THICKNESS TO BE .062 +/- .005 INCH  
WITH 2 OZ. COPPER ON TWO OUTER LAYERS AND  
1 OZ. COPPER ON TWO INTERNAL LAYERS.  
FLAMMABILITY RATING: 94 V-0 MINIMUM.
- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.  
0.00 ARE PRIMARY DATUMS.
- DRILLING: DRILL HOLES PER SCHEDULE. PLATE THROUGH  
HOLES WITH COPPER, .001 INCH THICK MIN. ALL  
HOLE SIZES ARE SPECIFIED AFTER PLATING.  
HOLE LOCATION TOLERANCES ARE +/- .003  
INCH IN RELATION TO CENTER
- FINISH: SMOBC USING WET MASK, OR LPI BOTH SIDES, COLOR GREEN.  
SILKSCREEN BOTH SIDES WITH WHITE NON-CONDUCTIVE INK.  
GOLD IMMERSION BOTH SIDES.
- CONTROLLED 100 OHM IMPEDANCE (AT 2.5 GHz FREQ.) FOR LAYER 1-2
- SUBJECT TO CHANGE BY MANUFACTURER, DEPENDING ON DIELECTRIC  
CONSTANT DEVIATIONS. PLEASE CONSULT LTC.
- DO NOT ALTER ARTWORK TO ADD LOGO OR DATE CODE,  
MAY MODIFY PAD SIZE TO MEET END FINISH.
- SCORING: (NOT REQUIRED FOR PROTOTYPE BOARDS)



UNLESS OTHERWISE SPECIFIED		APPROVALS		TECHNOLOGY	
DIMENSIONS ARE IN INCHES TOLERANCES: 0.XX" = ±0.01" 0.XXX" = ±0.005" INTERPRET DIM AND TOL PER ASME Y14.5M-1994 THIRD ANGLE PROJECTION		PCB DES.	AK	1830 MCCARTHY BLVD MILPITAS, CA 95035 PH: (408)432-1900 www.linear.com LTC CONFIDENTIAL- FOR CUSTOMER USE ONLY	
		APP ENG.	MARK T.		
				TITLE: FABRICATION DRAWING	
				ADC LOGIC PROBE ADAPTER BOARD	
				SIZE	IC NO.
				N/A	DEMO CIRCUIT 1321A
				SCALE = NONE	REV 2
				FILENAME: DC1321A-1.PCB	SHT 1 OF 1